PNP Silicon Epitaxial Transistor

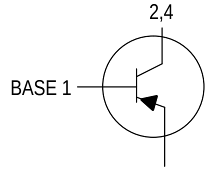
PZT2907AT1

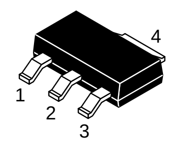
Motorola Preferred Device

**SOT-223 PACKAGE
PNP SILICON
TRANSISTOR
SURFACE MOUNT**

This PNP Silicon Epitaxial transistor is designed for use in linear and switching applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

- NPN Complement is PZT2222AT1
- The SOT-223 package can be soldered using wave or reflow
- SOT-223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Available in 12 mm tape and reel
  Use PZT2907AT1 to order the 7 inch/1000 unit reel.
  Use PZT2907AT3 to order the 13 inch/4000 unit reel.





**CASE 318E-04, STYLE 1
TO-261AA**

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	–60	Vdc
Collector-Base Voltage	V_{CBO}	–60	Vdc
Emitter-Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current	I_C	–600	mAdc
Total Power Dissipation @ T_A = 25°C(1) Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction-to-Ambient (surface mounted)	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625″ from case Time in Solder Bath	T_L	260 10	°C Sec

DEVICE MARKING

P2F

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = –10 μAdc, I_E = 0)	$V_{(BR)CBO}$	–60	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	–60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = –10 μAdc, I_C = 0)	$V_{(BR)EBO}$	–5.0	—	—	Vdc
Collector-Base Cutoff Current (V_{CB} = –50 Vdc, I_E = 0)	I_{CBO}	—	—	–10	nAdc
Collector-Emitter Cutoff Current (V_{CE} = –30 Vdc, V_{BE} = 0.5 Vdc)	I_{CEX}	—	—	–50	nAdc
Base-Emitter Cutoff Current (V_{CE} = –30 Vdc, V_{BE} = –0.5 Vdc)	I_{BEX}	—	—	–50	nAdc

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS[2]					
DC Current Gain	h_{FE}				—
(I_C = –0.1 mAdc, V_{CE} = –10 Vdc)		75	—	—	
(I_C = –1.0 mAdc, V_{CE} = –10 Vdc)		100	—	—	
(I_C = –10 mAdc, V_{CE} = –10 Vdc)		100	—	—	
(I_C = –150 mAdc, V_{CE} = –10 Vdc)		100	—	300	
(I_C = –500 mAdc, V_{CE} = –10 Vdc)		50	—	—	
Collector-Emitter Saturation Voltages	$V_{CE(sat)}$				Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)		—	—	–0.4	
(I_C = – 500 mAdc, I_B = –50 mAdc)		—	—	–1.6	
Base-Emitter Saturation Voltages	$V_{BE(sat)}$				Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)		—	—	–1.3	
(I_C = –500 mAdc, I_B = –50 mAdc)		—	—	–2.6	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = –50 mAdc, V_{CE} = –20 Vdc, f = 100 MHz)	f_T	200	—	—	MHz
Output Capacitance (V_{CB} = –10 Vdc, I_E = 0, f = 1.0 MHz)	C_c	—	—	8.0	pF
Input Capacitance (V_{EB} = –2.0 Vdc, I_C = 0, f = 1.0 MHz)	C_e	—	—	30	pF
SWITCHING TIMES					
Turn-On Time (V_{CC} = –30 Vdc, I_C = –150 mAdc, I_{B1} = –15 mAdc)	t_{on}	—	—	45	ns
Delay Time	t_d	—	—	10	
Rise Time	t_r	—	—	40	
Turn-Off Time (V_{CC} = –6.0 Vdc, I_C = –150 mAdc, I_{B1} = I_{B2} = –15 mAdc)	t_{off}	—	—	100	ns
Storage Time	t_s	—	—	80	
Fall Time	t_f	—	—	30	

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle = 2.0%.

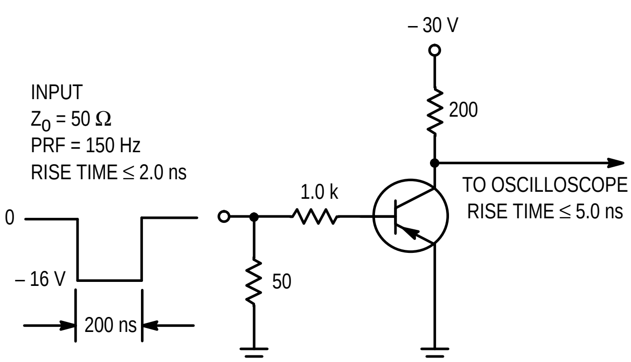


Figure 1. Delay and Rise Time Test Circuit

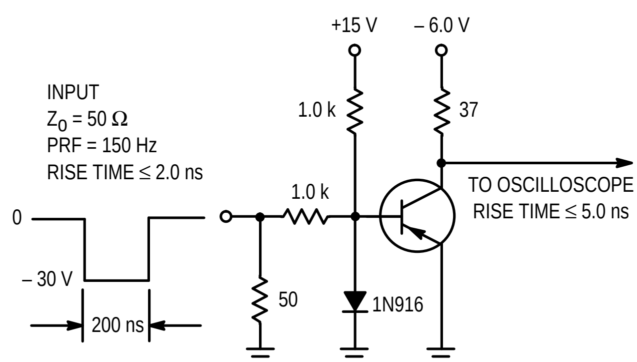


Figure 2. Storage and Fall Time Test Circuit

TYPICAL ELECTRICAL CHARACTERISTICS

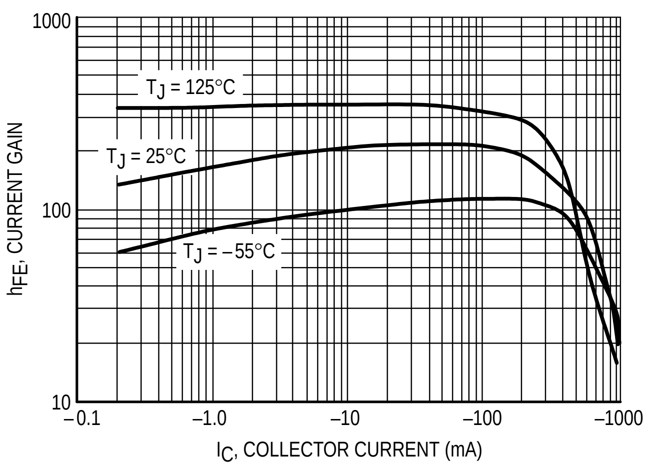


Figure 3. DC Current Gain

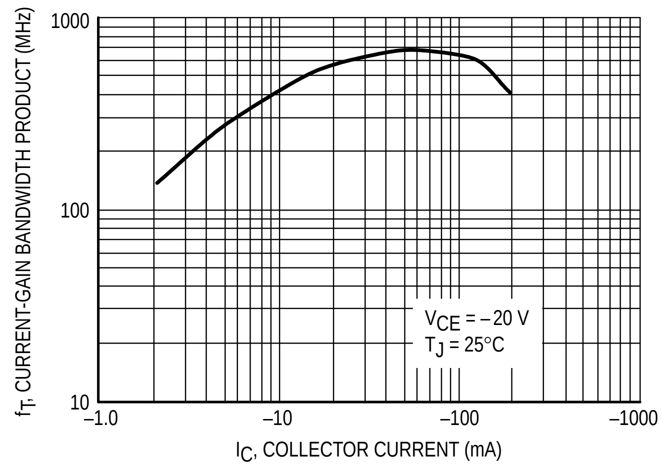


Figure 4. Current Gain Bandwidth Product

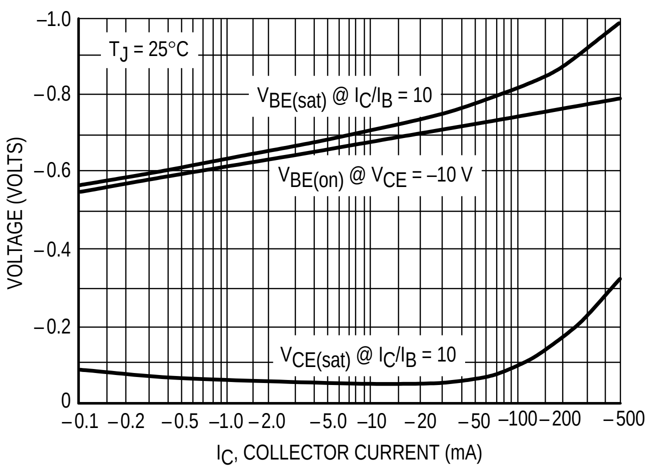


Figure 5. “ON” Voltage

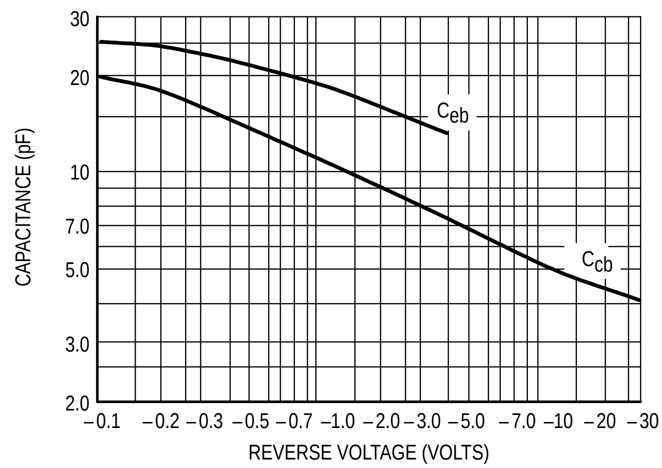


Figure 6. Capacitances

INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet for the SOT-223 package, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150°C - 25°C}{83.3°C/W} = 1.5 \text{ watts}$$

The 83.3°C/W for the SOT-223 package assumes the recommended collector pad area of 965 sq. mils on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. If space is at a premium, a more realistic approach is to use the device at a P_D of 833 mW using the footprint shown. Using a board material such as Thermal Clad, a power dissipation of 1.6 watts can be achieved using the same footprint.

MOUNTING PRECAUTIONS

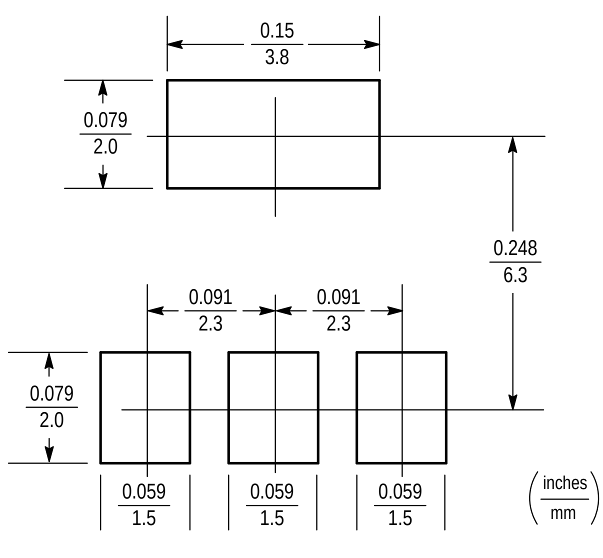
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

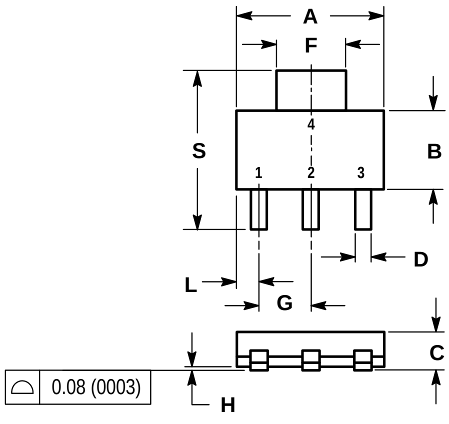
* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

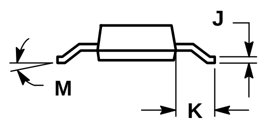
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



PACKAGE DIMENSIONS





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

CASE 318E–04
ISSUE H
TO-261AA

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